# Low-cost, high-resolution A/D Conversion with an 8-bit Microcontroller

## *Introduction*

The COP8ACC is a new member of National Semiconductor's 8-bit microcontroller family COP8™. The device is manufactured in M$^2$CMOS technology and has been designed using National's "Configurable Controller Methodology (CCM)". CCM allows for the rapid and reliable development of new microcontroller derivates based on a fully qualified and verified mega-cell library. The new COP8ACC integrates several features that make this microcontroller the ideal choice for all applications requiring a fast, high-resolution A/D converter at a low cost. This paper describes how the integrated functional blocks can be used to implement an up to 16-bit resolution single-slope A/D converter. The 28 pin package supports 6 A/D channels and the 20 pin package 4 channels. Compared to similar single-slope implementations the A/D conversion time has been improved by a factor of ten.

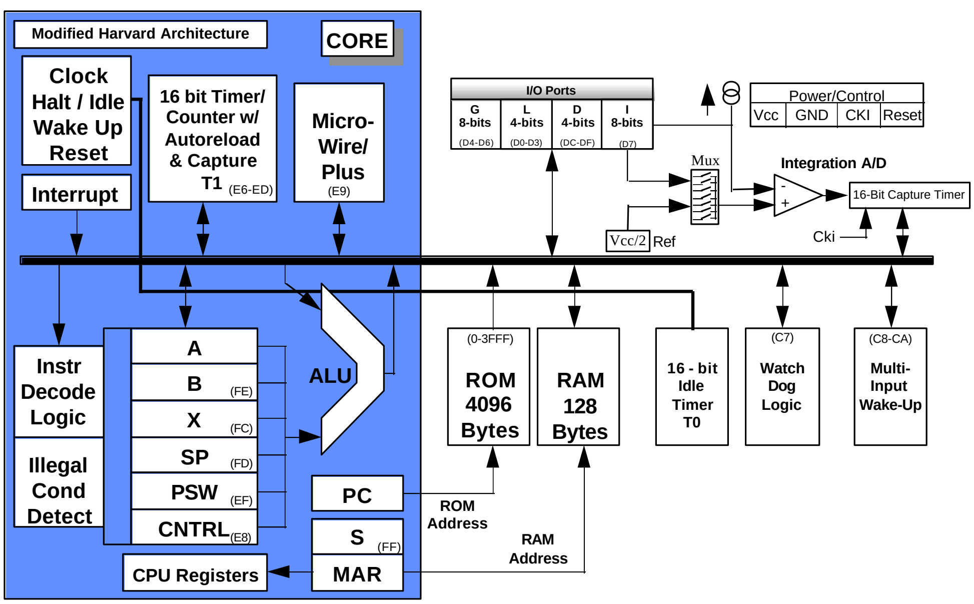


Figure 1: COP8ACC block diagram

The first section  provides an overview of the COP8ACC features and peripheral functions, before discussing the A/D implementation in detail in the next section.

## COP8ACC Feature Overview

Figure 1 shows the COP8ACC block diagram. The following paragraphs give an overview of the main features and key parameters of the microcontroller

### CPU & instruction set

The COP8™ “feature core” is a modified Harvard architecture, which allows the transfer of data between program memory and data memory. The minimum instruction cycle time is 1 µs. 77% of the instructions are single cycle and single byte. Eight  interrupt vectors are supported by the COP8ACC and two indirect data memory pointers are available.

### Peripheral functions

#### *Analog function block*

The COP8ACC has an analog fucntion block, that allows the designer to implement a fast, high resolution A/D conversion at a low cost. In the next chapter this block is covered in more detail. It consists of:

- Analog comparator
- Analog multiplexer with 7 inputs
- Constant current source
- Vcc/2 voltage reference
- Fast 16-bit capture timer with “auto-reset at start” function

#### *Timer T0*

The free running 16-bit timer T0 supports underflow periods of 4k, 8k, 16k, 32k and 64k instruction cycles. An underflow can trigger an interrupt and sets a status bit, which can also be polled by software. Timer T0 is also used in the IDLE power save mode to periodically wake-up the microcontroller after a programmed time period.

#### *Timer T1*

Timer T1 of the COP8ACC is a 16-bit multifunction timer with two associated 16-bit autoreload/capture registers. The timer supports three programmable operating modes:

- Processor independent PWM (pulse width modulation)
- External event counter with programmable edge
- Capture mode, which supports frequency or time measurements with two independent inputs and programmable edges

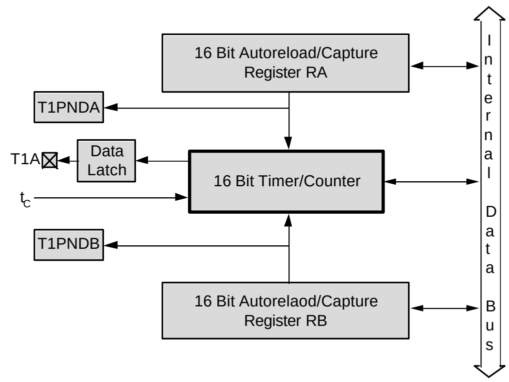


Figure2: Timer T1 PWM mode

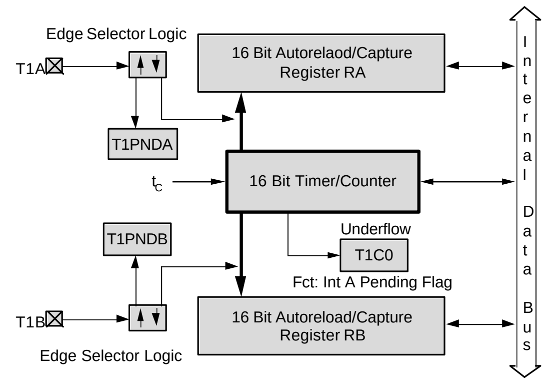


Figure 3: Timer T1 frequency/time measurement

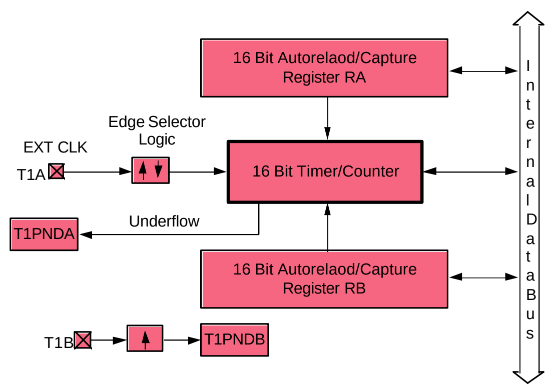


Figure 4: Timer T1 event counter mode

## *Multi-Input-Wake-Up*

Up to 4 multi-input-wake-up (MIWU) input/outputs provide the possibility to wake-up the microcontroller via external events from the HALT and IDLE power save modes (e.g. depression of any key in a keyboard matrix using the MIWU pins.) The polarity of the input signal is programmable, in addition a programmable external interrupt can be associated with each MIWU signal.

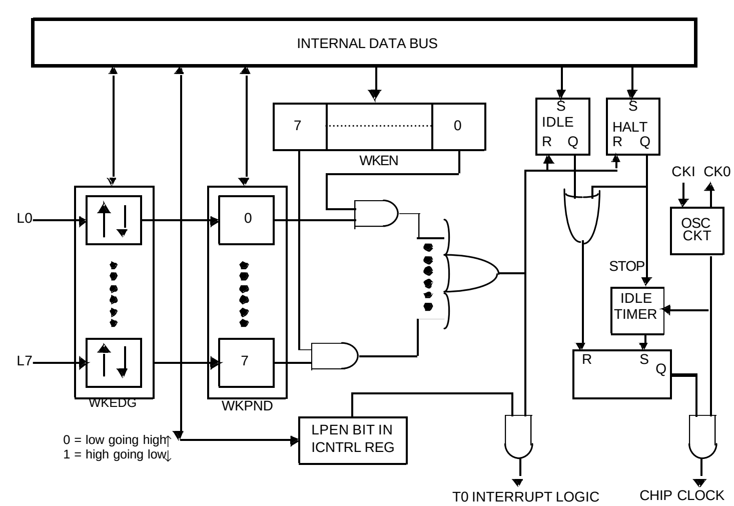


Figure 5:Multi-Input-Wake-Up

***Serial Interface***

The on-chip peripheral functions are complemented by MICROWIRE/PLUS™, a serial, SPI compatible, 3-wire interface, which allows for the easy connection of external peripherals to the microcontroller (EERAM, LCD drivers, National audio devices (equalizer, tone controls, etc.)) Microwire supports data rates up to 5 MBps.

**Program and Data Memory**

The COP8ACC comes with 4096 bytes ROM program memory and 128 bytes RAM data memory. An OTP (One-Time-Programmable) version with 4k EPROM program memory is available as well.

**Inputs and Outputs**

The D-Port outputs of the COP8ACC can sink 15mA and can therefore be used to direct drive LEDs and Triacs. Several of the pins can be tied in parallel to increase the possible sink current. The I/Os are individually software configurable, i.e. each single pin can be programmed to be either a "weak-pullup" input, high impedance (Hi-Z) input, "push-pull 1" or "push-pull 0", output. The actual pin status can be read back indepent of the pins programmed state, which allows for the easy detection of external shorts or open connections.
Schmitt-Trigger inputs on ports G and L, increase the reliable signal detection even in noisy environments.

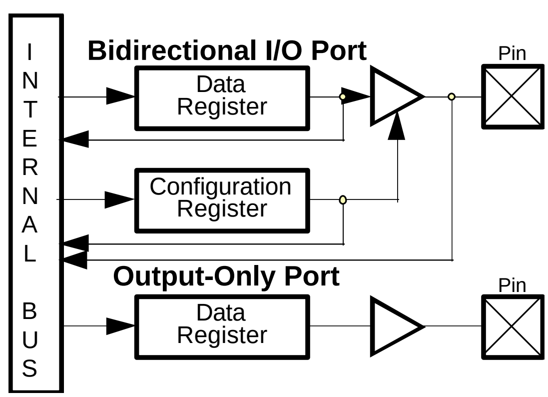


Figure 6: COP8 I/O block diagram

**Power Save Modes**

COP8™ microcontrollers support two power save modes: HALT and IDLE. The fully static CMOS design allows to stop all processor activities, including the oscillator in HALT mode. Current consumption decreases to typical values of 1 uA in HALT mode.

In IDLE mode only the idle timer TO and the oscillator are active. Current consumption in this mode is reduced to about 1/3 of the value in normal operation.

A wide operating voltage range from 5.5V down to 2.5V allows for further reductions in power consumption by lowering the operating voltage.

**Packages and Temperature Ranges**

The COP8ACC is available in 28 pin DIL and SO, and in 20 pin SO packages.
The controller is offered in two different temperature ranges:

- Commercial (0°C....+70°C)
- Industrial (-40°C....+85°C)

**Safety and Reliability Aspects**

All microcontrollers of the COP8 family have implemented a non-maskable “software trap” interrupt. This feature allows the programmer to do a self-recovery in software after illegal operating conditions, which could for example be caused by disturbances in noisy environments, drops in power supply, but also by undiscovered bugs in the software. Those illegal operating conditions are: Access to unused program memory, access to programm memory addresses exciting the physically implemented memory, access to physically unavailable RAM addresses, over push or pop of the stackpointer.

The COP8ACC also has an integrated WATCHDOG™ and clock monitor. The watchdog is not only triggered, like in most microcontroller implementations, by a “non-service” within a maximum time period (timeout), but also by too frequent watchdog services. By this measure it is assured that even the condition, “stuck in an endless loops which happens to do a valid watchdog service” can be detected. The clock monitor switches the microcontroller into a defined Reset state (all I/Os at defined level) if the main oscillator fails.

The modified Harvard architecture allows for the calculation of a program memory checksum, which is for example in the USA mandated by Underwriters Laboratories spec UL 1998 for safety critical microcontroller applications.

The pinstatus of all COP8 I/Os can be read back independently of their programmed state. Using this feature exeternal shorts or open connections can be reliably detected (also a requirement of the UL1998 spec).

A patented ESD (electro static discharge) protection circuit enables the COP8ACC to withstand better than 5000V of ESD (juman body model). The device is 99% faultgraded, meaning that 99% of all possible “stuck at 1” and “stuck at 0” faults inside the chip can be detected during final production test. By this, even the most rigid quality requirements, are exceeded. (automotive industry mandates 95% for example).

National Semiconductor’s patented EMI (electromagnetic interference) reduction technique, minimizes the COP8ACC’s radiated emissions. Figure 7 and 8 show the EMI of an 8-bit microcontroller without EMI reduction and of a COP8 microcontroller with integrated EMI reduction circuitry.

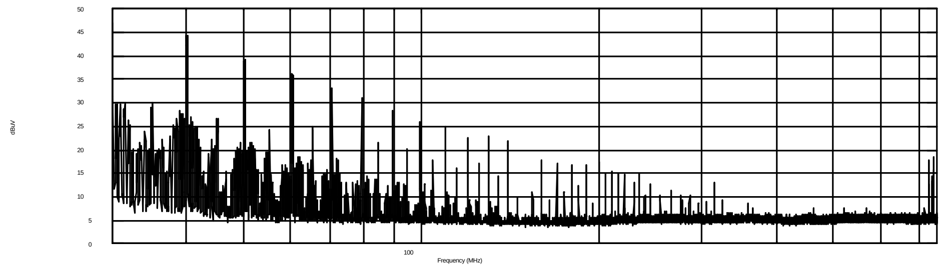


Figure 7: Microcontroller without EMI reduction

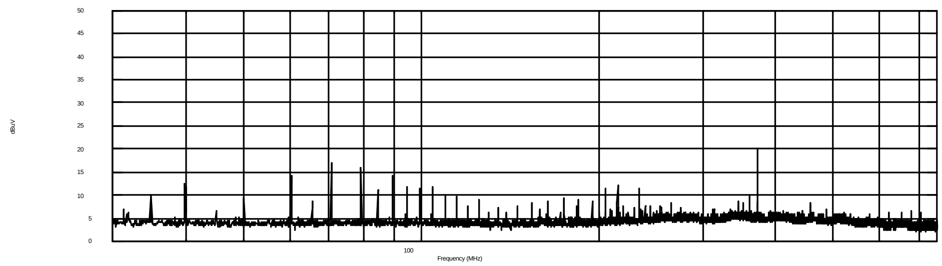


Figure 8: COP8™ Microcontroller with patented EMI reduction circuitry

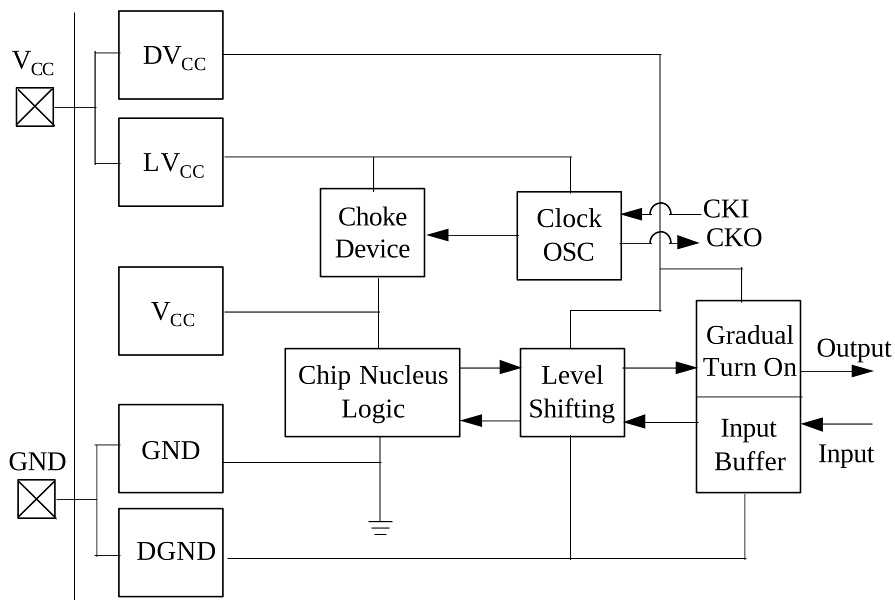


Figure 9: COP8™ EMI reduction circuit block diagram

## *A/D Conversion*

**Single-Slope A/D Implementation**

An analog function block integrated on the COP8ACC. The block diagram is shown in Figure 10.

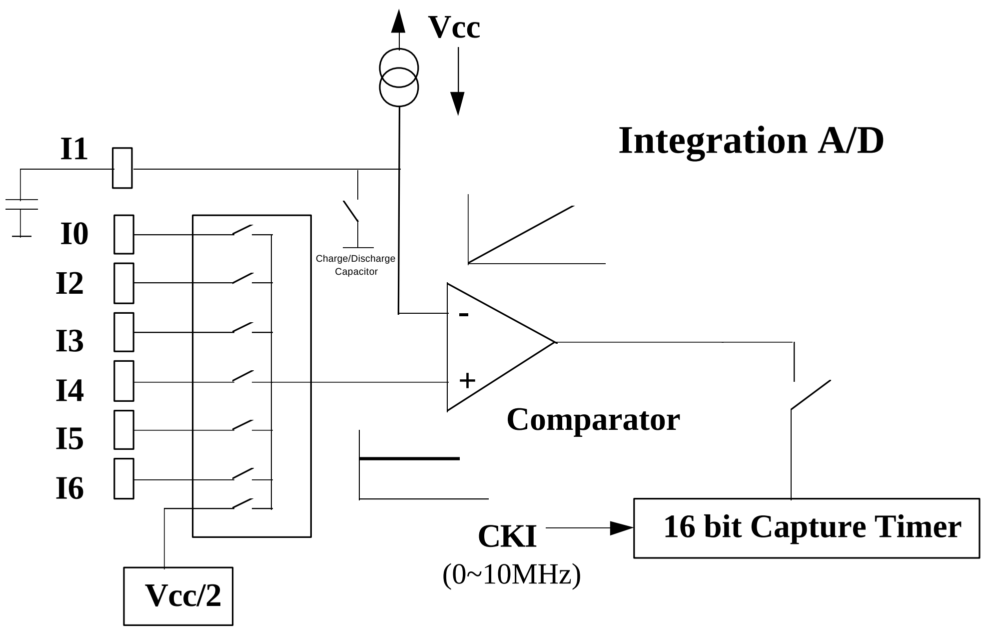


Figure 10: COP8ACC analog function block

The negative input of the comparator is connected to one of the microcontroller I/O pins (I1). The same pin is also connected to the on-chip constant current source, which can be enabled and disabled under software control. To implement a single-slope A/D converter, the only required external component is a capacitor, which is connected to the output of the constant current source (negative comparator input) I1.

The positive comparator input is connected to a seven-to-one analog mulitplexer. Six of the multiplexer inputs are connected to input pins of the COP8ACC, the seventh is connected to the integrated Vcc/2 voltage reference.

The output of the comparator goes to the trigger input of a fast 16-bit capture timer, which is clocked with the external oscillator frequency (100ns max.).

Up to six analog voltages are connected to the input pins of the COP8ACC and are, software selected via the analog multiplexer, connected to the positive comparator input.

To initiate an analog to digital conversion, the constant current source is enabled by software. The next step is to discharge the external capacitor, by programming pin I1 as a “0”-output (switch to ground). Having the constant current source enabled during discharging is not a problem, as the constant current is small enough to not cause a noticeable voltage drop over the transistor switch to ground. This is, on the contrary, the recommended order, to allow the constant current source sufficient time to stabilize, before doing a conversion. The input with the analog voltage to be measured is now selected via the analog multiplexer.

As a next step charging of the external capacitor is started, by opening the transistor switch to ground under software control. At the same time the 16-bit upward counter is started. Starting the counter will automatically reset the counter to “0” (can be disabled in software if desired). The counter is now incremented with the external oscillator frequency.

As soon as the voltage over the capacitor reaches the same value as the applied analog voltage to be measured, the comparator output switches from “1” to “0”. This triggers a capture event and the counter value of the 16-bit up counter is stored. As the capacitor is charged with a constant current, the stored 16-bit counter value is directly proportional to the analog voltage applied to the positive comparator terminal.

**Calibration and Accuracy Considerations**

The internal Vcc/2 voltage reference of the COP8ACC can be used for self-calibration of the A/D in such cases where absolute measurement accuracy is not a major concern. The voltage reference I implemented as a matched resistor voltage divider with a maximum variance of +-40mV. However, on top of this variance any tolerances in the microcontroller’s voltage supply are added. If the microcontroller is for example operated with a 5 V voltage regulator that has a +-5% output accuracy, a worst case tolerance of the Vcc/2 reference results, which is: 2.5V +- (40mV+250mV), so that reference voltages between 2.21V and 2.89V can result. Using a voltage regulator with a 1% tolerance will improve the resulting reference voltage to a range between 2.41V and 2.59V.

Applications requiring a better absolute accuracy, should use an external precision voltage reference, which can be permanently connected to one of the analog inputs. Another possibility is the end-of-line calibration, where a precise reference voltage is applied to one of the analog inputs, is read by the microcontroller software and then stored as a permanent reference value in an external EERAM memory. In applications requiring EERAM memory anyway to also store other parameters, this approach offers the best compromise between cost and achievable accuracy.

The achievable accuracy depends also on the linearity of the capacitor’s charge ramp, the absolute variance of the constant current source, the common mode range of the comparator, and the quality of the external capacitor. Best results are achieved with high quality plastic or polyester capacitors. The constant current source itself has a supply voltage dependent variance (condition: Vcc =5V+-10%) of only +-2uA, lower supply voltage variations result also in a lower variation of the constant current. The analog input voltage should, in order to not exceed the common mode range of the comparator, stay below a maximum voltage of Vcc-1.5V.

Taking all of above described factors into account, it is possible to achieve an absolute linearity error of less the 1% over the entire measurement range.

**A/D Resolution and Conversion Time**

Resolution and conversion time, which can be achieved with the single-slope approach, depend on the value of the external capacitor, the analog input voltage range, the value of the constant current, and the oscillator frequency of the microcontoller. A nice benefit of the single-slope approach is the possibility to trade-off resolution via conversion speed and vice versa. This is simply achieved by changing the value of the external capacitor.

Due to process variances the value of the constant current can vary from lot to lot between a minimum value of 7µA and a maximum of 32µA. To calculate the minimum achievable resolution for a given capacitor value, analog input voltage range and oscillator frequency, the following formula can be used:

$$CaptureTimerValue = \frac{C * dV}{I_{MAX} * t_{CLK}}$$

with:

| | |
|---|---|
| C | = capacitor value |
| dV | = analog input voltage range |
| $I_{max}$ | = maximum constant current (32µA) |
| $t_{CLK}$ | = oscillator cycle time |

Example:

| | |
|---|---|
| C | = 10nF |
| dV | = 3.5V |
| $I_{max}$ | = 32µA |
| $t_{CLK}$ | = 100ns (10MHz clock) |

$$CaptureTimerValue = \frac{10 \cdot 10^{-9} * 3.5}{32 \cdot 10^{-6} * 100 \cdot 10^{-9}} = 10937$$

A counter value for 10937 equates a minimum resolution (worst case) of 14 bits. Reducing the oscillator frequency by half or doubling the capcitor value will reduce the A/D resolution by 1 bit.

The longest possible conversion time results if the external capacitor is charged with the minimum constant current ($I_{min}$ = 7µA). Replacing $I_{max}$ with $I_{min}$ in above formula results in a counter value of 50000 with our example values, which equates to a best-case resolution of 16-bit. With a 10MHz chip-oscillator frequency, the capture timer is clocked with 100ns. Therefore the maximum (worst case) A/D conversion time in this example is:

$$T_{max} = 50000 * 100ns = 5.0ms$$

Faster conversion times, while at the same time reducing A/D resolution, can be achieved by using a smaller capacitor value. Reducing in above example the capacitor value by a factor of 10, will result in a minimum resolution of 11 bit and a maximum conversion time of 500µs (i.e., the conversion time is also reduced by a factor of 10).

**Summary**

After National Semiconductor introduced with the COP88EK the world's first 8-bit microcontroller with high-resolution, single-slope A/D support to the market, this concept is enhanced with the COP8ACC to a new level of performance. The COP8ACC's conversion time has been accelerated by a factor of 10. With this, the COP8ACC can also handle applications that require relatively fast conversion speeds. A 11 bit conversion just takes 500µs, an 8-bit conversion just 30µs. Nevertheless is the price of a COP8ACC in a region, where so far only microcontrollers with 8-bit A/D converters can be found (~$2.50 for 10kU ROM version). The extremely low electromagnetic emissions of the controller can result in considerably lower overall system cost, as external components for EMI filtering to meet CE regulations are no longer required. The flexible input/output structure with multi-input-wake-up, Schmitt triggers and individually programmable pins, as well as the powerful 16-bit timer, allow for further reductions in external component count. Additional system functions requiring so far additional circuitry can be handled by the microcontroller, allowing the designer to meet ever more aggressive price targets without sacrificing performance or functionality.